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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,753	06/20/2005	Tsuyoshi Yamamoto	8013-1242	6354

466 7590 06/23/2011

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EXAMINER	
NGUYEN, TRUNG Q	
ART UNIT	PAPER NUMBER
2858	

NOTIFICATION DATE	DELIVERY MODE
06/23/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

DocketingDept@young-thompson.com

Office Action Summary	Application No.	Applicant(s)	
	10/539,753	YAMAMOTO ET AL.	
	Examiner	Art Unit	
	TRUNG NGUYEN	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-19* is/are allowed.

6)☒ Claim(s) *20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06202005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claim 20 is are rejected on the ground of nonstatutory double patenting over claim 1 of U. S. Patent No. 7,443,720 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The instant application claim is broader in every aspect than the patent claim and is therefore an obvious variant thereof . The application are claiming common subject matter, as follows:

Claims of Instant Application	Claims of U.S. Patent No. 7,443,720
20	1

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (U.S. 7,145,170) in view of Astafiev et al. (U.S. 7,443,720).

Yamamoto et al. disclose in Fig. 2, extracting an excess Cooper-pair existing in a quantum box (see claim 1, column 4, lines 30-54, wherein first and second superconducting charge quantum bit devices, each includes a quantum box electrode comprising a superconductor, a counter electrode coupled to the quantum box electrode through a tunnel barrier, and a gate electrode coupled to the quantum box electrode through a gate electrostatic capacitor) electrode to a trap electrode of a quantum computing device when a bias voltage is applied to the quantum computing device (see claim 10, also column 1, lines 35-55); and measuring a change of a current value flow (see column 5, lines 10-64), which includes an island electrode coupling with the trap electrode through a readout capacitance (capacitance 105 and 205 are coupled to the two cooper pair boxes), before and after the extracting of the excess Cooper-pair (103 & 203) . Yamamoto et al. did not clearly disclose the measuring a change of a current value flowing in a single electron transistor. However, Astafieve et al. disclose a single electron transistor (20). Therefore, it would have been obvious to one of ordinary skill in

the art, at the time the invention was made, to combine the feature taught by Astafiev et al. to the disclosure by Yamamoto et al. so that sensitivity of the single electron transistor is increased in order to measure the readout capacitance which couples the trap electrode and the island electrode must be conducted by considering suppression of the runnel current between the trap electrode and the island electrode, and securement of high sensitivity of the single electron transistor.

Reasons for Allowance

2. Claims 1-19 are allowed.

The following is an examiner's statement of reasons for allowance:

Claims 1-9 recite inter alia, "a first gate electrode coupling with the quantum box electrode through a static capacitance; a trap electrode coupling with the quantum box electrode through a second tunnel barrier; and a single electron transistor, wherein the single electron transistor, further comprising a source electrode, drain electrode, an island electrode, and a second gate electrode coupling with the island electrode, wherein the trap electrode and the island electrode of the single electron transistor being coupled through a readout capacitance."

Claims 10-19 recite inter alia, "a single electron transistor comprising a source electrode, a drain electrode, an island electrode, and a gate electrode coupling with the island electrode through a gate capacitance; and a trap electrode coupling with the

island electrode through a readout capacitance as well as coupling with a quantum box electrode of the quantum computing device through a tunnel barrier."

The art of record does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include the above limitations.

Conclusion

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Trung Nguyen** whose telephone number is **(571) 272-1966**. The examiner can normally be reached on Monday through Friday, 9:00AM – 5:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Huy Phan** can be reached at *(571) 272-7924*.

Examiner: Trung Nguyen-Art 2858
June 16, 2011.

/HUY Q PHAN/
Supervisory Patent Examiner, Art Unit 2858